

REMARKS

Claims 36-47 have been added. No new matter has been introduced by way of this change.

It is respectfully submitted, for the reasons set forth below, that all the claims should be allowed and the application passed to issue.

Rejections under 35 U.S.C. § 103

The Examiner rejected claims 1-35 under 35 U.S.C. § 103(a) as being unpatentable (obvious) over U.S. Patent No. 5,444,663 issued to Furuno et al (herein "Furuno") in view of U.S. Patent No. 6,157,222 issued to Yaklin (herein "Yaklin"). These rejections are respectfully traversed.

It is respectfully submitted that a *prima facie* case of obviousness, as required under 35 U.S.C. § 103(a), has not been made for claims 1-35 and so the rejection is erroneous as to claims 1-35 for at least the reasons set forth below.

In regard to claim 1, it is respectfully submitted that, for the reasons set forth below, the teachings of Furuno may not legitimately be combined with those of Yaklin, and thus the Examiner has used impermissible hindsight to reconstruct the invention from the teachings of Furuno and Yaklin. For example, the Examiner has written "... *it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide voltage detector of Furuno with the selectable threshold point circuit of Yaklin in order to provide a constant voltage to an internal circuit of IC during testing/normal operation.*" (emphasis added) (Office Action, p. 3, lines 3-6).

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

3 EMBARCADERO CENTER
SUITE 2800
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

But the Examiner has not shown that Yaklin discloses, teaches or renders obvious a ***selectable threshold point circuit***. None of the features identified by the Examiner as a ***selectable threshold point circuit*** i.e. “[fig. 5 or 7 or 8 or 10]” of Yaklin are a ***selectable threshold point circuit***. Yaklin characterizes his figures 5, 7, 8 as various kinds of comparator (Yaklin, col. 3, lines 31-33 and 37-42). Yaklin further characterizes his figure 10 as a CNA (Cable not-active circuit) made up of the comparator of figure 5 (Yaklin, col. 9, lines 16-17) and a circuit to select a signal from a choice of the signal of interest V_{SI} and a calibration reference signal V_{REF} . Selecting a signal as in Yaklin (Yaklin, col. 9, lines 44-48) is distinct from selecting a threshold level as in the invention. Comparators as in Yaklin are distinct from selectable threshold point circuits in the art.

Even if one were to assume, purely for the sake of argument, that the comparators of Yaklin were selectable threshold point circuits as the Examiner suggests, there would be no motivation to use them ***to provide a constant voltage*** as recited by the Examiner. This is because the comparators of Yaklin do not provide a constant voltage; they provide a binary output logic signal (Yaklin, col. 5, lines 36-37). Indeed Yaklin is completely silent as to any constant voltage except V_{REF} which is an externally supplied signal of unspecified origin (Yaklin, col. 8, lines 41-42).

Thus, for the various reasons cited above, it is not proper to combine the teaching of Yaklin with those of Furuno, and a *prima facie* showing of obviousness has not been made.

It should also be noted that the present specification identifies **any need for** a constant (or reference) voltage as a **deficiency** in the prior art (p. 2, lines 10-15) that the invention overcomes. Thus, even if one supposes, for the sake of argument, that **to provide a constant voltage** were enabled by Yaklin, then the use of a constant voltage in Furuno (and the purported use in Yaklin) teach away from the invention. Art that teaches away from the

invention also teaches away from a finding of obviousness over that art and thus, for this additional reason, a finding of obviousness is not supported.

Moreover, even if it were legitimate to combine all the teachings of Yaklin and Furuno, they do not, either alone or in combination, teach, suggest or render obvious all the limitations of claim 1. For example, claim 1 recites, in part, "...a *selectable threshold point circuit connected to the voltage following circuit* ...". It is respectfully submitted that neither Yaklin nor Furuno, separately or in combination, teaches, discloses or suggests a selectable threshold point circuit connected to a voltage following circuit. Figure 2 of Furuno shows that the voltage following circuit (voltage follower) of Furuno is **not** coupled to the selectable threshold point circuit (supply voltage decision circuit) of Furuno. And this deficiency would not be cured by substituting "*the selectable threshold point circuit of Yaklin in order to provide a constant voltage*" as suggested by the Examiner (Office Action, p. 3, lines 4-6).

Thus, it is respectfully submitted that, for the various reasons laid out above, there has been no *prima facie* showing of obviousness and claim 1 is allowable under 35 U.S.C. § 103(a).

Moreover, claims 2-15 depend, directly or indirectly, upon claim 1 and are thus allowable for at least the same reasons as claim 1.

As to claim 21, the Examiner has made essentially the same arguments as for claim 1 and has offered no further motivation for combining the teaching of Furuno with those of Yaklin. Thus, it is respectfully submitted that claim 21 is allowable for substantially the same reasons as claim 1, including that:- (1) It is not proper to combine the teaching of Furuno with those of Yaklin. (2) Furuno and Yaklin each teach away from the invention. And (3) even in (impermissible) combination, Furuno and Yaklin combined do not teach, disclose, suggest or

render obvious all the limitations of claim 21, for example, the connection of a selectable threshold point circuit to a voltage following circuit (claim 21, lines 8-9).

A further example of how, even combined, Furuno and Yaklin do not teach, disclose, suggest or render obvious all the limitations of claim 21, follows. Claim 21 recites, in part, “*A system comprising: a memory; a microprocessor; and ...*”. The Examiner has written (Office Action, p. 3, lines 7-9) “*Regarding claim 21, Furuno discloses: A system [fig. 1], a memory [see fig. 13]; a microprocessor [see fig. 13] and ...*”. But Furuno characterizes “*FIG. 1 is a block diagram of an EPROM...*” and “*FIG. 13 is a block diagram showing a microcomputer system in which EPROM according to the present invention is mounted*” (Furuno, col. 2, lines 32-32 and 56-58). Thus, Furuno expressly calls out that the EPROM (or system) of FIG.1 is **mounted within** the system (or memory and microprocessor) of FIG. 13. The Examiner has proposed Furuno discloses essentially the opposite, i.e., system **comprising** microprocessor and memory (rather than the system **comprised within** microprocessor and/or memory that Furuno actually discloses).

Thus, it is respectfully submitted that, for the various reasons laid out above there has been no *prima facie* showing of obviousness, and claim 21 is allowable under 35 U.S.C. § 103(a).

Moreover, claims 22-35 depend, directly or indirectly, upon claim 21 and are thus allowable for at least the same reasons as claim 21.

As to independent method claim 16, the Examiner has written, “... *clearly the above discussion of Furuno in view of Yaklin will provide the recited method*”. It is respectfully submitted that claim 16 is allowable for substantial reasons including that:- (1) It is not proper to combine the teaching of Furuno with those of Yaklin, and (2) Furuno and Yaklin each

teach away from the invention, as argued for claim 1 above. Moreover, the Examiner has not pointed out how the limitations of claim 16 are anticipated by Furuno and Yaklin separately or even in (impermissible) combination. For example, claim 16 contains limitations as to selecting, tracking and generating not shown to be found in the prior art and therefore no *prima facie* case for obviousness under 35 U.S.C. § 103(a) has been made. For the reasons set forth above, reconsideration and allowance of claim 16 is respectfully requested. Claims 17-20 depend, directly or indirectly, upon claim 16, and allowance of claims 17-20 is respectfully requested for at least the same reasons as claim 16.

Therefore, it is requested that the Examiner reconsider and withdraw the rejections and allow claims 1-35.

Newly presented claims

Claims 36-47 have been added to further define the invention. It is respectfully submitted that new claims 36-47 are fully supported by the application as filed, directed to the same invention and do not introduce any new matter. Entry into the record, consideration and allowance are respectfully requested.

SUMMARY

Claims 1-35 were pending at last examination. Claims 1-35 were rejected. Claims 36-47 have been added. It is respectfully requested that the examiner consider the newly presented claims, reconsider the rejected claims, withdraw the rejections and pass this case to issue with all of pending claims 1-47 allowed.

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

3 EMBARCADERO CENTER
SUITE 2800
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

If the Examiner believes it could serve to advance the case, then the examiner is invited to call the undersigned at 415-217-6000 (PST).

EXPRESS MAIL LABEL NO.:

EV 212 982 448 US

Respectfully submitted,



N.R.H. Black
Agent
Reg. No. 43,320

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

3 EMBARCADERO CENTER
SUITE 2800
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

A1

36. (New) A voltage detector energized by a supply voltage, the detector comprising:

a plurality of control signal terminals receiving a plurality of control signals;

a selectable threshold point circuit comprising a plurality of reference current sources connected to a common circuit node, each reference current source operable to conduct a respective reference current magnitude and to be controlled by a respective control signal;

a transistor having a current terminal connected to the common circuit node and further having a control terminal controlled by the supply voltage, the transistor operable to conduct a switch current having a switch current magnitude responsive to a magnitude of the supply voltage; and

an output terminal carrying an output signal responsive to a voltage at the common circuit node, a first state of the output signal corresponding to a first condition wherein the transistor acts to limit a sum of the reference current magnitudes, and a second state of the output signal corresponding to a second condition wherein the selectable threshold point circuit acts to limit the switch current magnitude, whereby the voltage detector detects a sufficiency of the supply voltage.

37. (New) A voltage detector energized by a supply voltage and comprising:

a selectable threshold point circuit operable to conduct a reference current having a selected one of a plurality of predefined current magnitudes through a circuit node in a first sense;

and

a switch circuit operable to conduct a voltage-controlled current through the circuit node in a sense opposite to the first sense, a magnitude of the voltage-controlled current being responsive to a magnitude of the supply voltage, the switch circuit further operable to generate an output indicating whether the supply voltage exceeds a threshold value responsive to whether the selected one of the plurality of predefined current magnitudes limits the voltage-controlled current.

38. (New) The voltage detector of Claim 37 wherein:
the a selected one of a plurality of predefined current magnitudes is selected in response to a plurality of control signals.

39. (New) The voltage detector of Claim 37 wherein:
the selectable threshold point circuit comprises a plurality of current mirror transistors.

40. (New) The voltage detector of Claim 39 wherein:
at least one of the current mirror transistors is coupled to a respective switch transistor controlled by a respective one of the control signals.

41. (New) The voltage detector of Claim 39 wherein:
at least two of the current mirror transistors have mutually different width-to-length ratios.

Cont
A1

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

3 EMBARCADERO CENTER
SUITE 2800
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

42. (New) The voltage detector of Claim 37 wherein:

the switch circuit consists essentially of a weak MOS transistor.

43. (New) A method for detecting a voltage level performed in a circuit, the method comprising:

selecting one of a plurality of amounts of current, the selected amount of current determining a selected value for a threshold point for a power supply;

tracking a voltage value of the power supply; and

generating an output that indicates whether the voltage value of the power supply has increased above or decreased below the selected value for the threshold point by determining whether the selected amount of current acts to limit a further current generated in response to the tracked voltage value of the power supply.

44. (New) The method of Claim 43 wherein selecting comprises transmitting at least one control signal to the circuit.

45. (New) The method of Claim 43 wherein selecting comprises turning on at least one switch transistor.

46. (New) The method of Claim 43 wherein generating comprises pulling a voltage level at a detecting node to ground when the value of the power supply exceeds the selected threshold point.

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

3 EMBARCADERO CENTER
SUITE 2800
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

*Conclud
A1*

47. (New) The method of Claim 43 wherein generating comprises pulling a voltage level at a detecting node to the value of the power supply when the value of the power supply is below the selected threshold point.

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

3 EMBARCADERO CENTER
SUITE 2800
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646